IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

FLYNN et al — Atty. Ref.: 550-466; Confirmation No. 7230

Appl. No. 10/691,501 — TC/A.U. 2189

Filed: October 24, 2003 — Examiner: Dinh, Ngoc V.

For: HARDWARE DRIVEN STATE SAVE/RESTORE IN A DATA PROCESSING SYSTEM

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October 31, 2008

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

REQUEST FOR RECONSIDERATION

Responsive to the Official Action dated August 1, 2008, reconsideration and allowance are respectfully requested.

Most of the claims 1-30 stand rejected under 35 U.S.C. §103 as allegedly being unpatentable based on newly-applied Woods in view of newly-applied Langford. This rejection is respectfully traversed.

Woods discloses an integrated circuit 130 in which state data is saved in a memory 270 that forms part of an interactive state power reduction manager (ISPRM) 160 as illustrated in Figure 2. The state data is serially scanned in and out of the memory 270 via the serial signal paths 234 and 232. The memory 270 used for state saving and state restoring is part of the ISPRM 160 and is not disclosed as the memory used during normal processing operation of the integrated circuit 130.

Langford discloses a system for increasing the speed of boundary scan test operations of an integrated circuit 10 by using existing address and data buses 14, 16 to transfer test data into the integrated circuit 10 for boundary scan and test results out of the integrated circuit following boundary scan. During the boundary scan test mode, the data inputs and data outputs of the integrated circuit are switched from the normal input and output connections, and a test word is input via the buses or a test response output via the buses using an external system data bus. See column 3, lines 9-17. This data transfer during testing is with an external testing circuit and not with the memory used during normal operation of the integrated circuit. This external system is the test processor referred to at the end of the Abstract.

There is no disclosure or suggestion in Langford of the test data flowing to or from the memory used in normal operation of the integrated circuit under test. Indeed, as would be appreciated by those skilled in this technical field, boundary scan testing performed as part of manufacture typically uses specialised external testing equipment which connects to the integrated circuit under test, applies a series of boundary scan signal patterns (test vectors), and recovers the test responses for checking against known correct responses. Because this testing is performed at manufacture, the test processor is not built into the integrated circuit.

The Examiner maps the claimed memory to the memory 270 of Woods. The independent claims specify that the multi-bit wide system bus transfers "multi-bit data words between said circuit and said memory ... during normal processing operation of said circuit and said memory." This is not the case with Woods in which the memory 270 is a special purpose memory (see column 7, lines 21-32) provided for the purpose of save and restore and is not the memory used during normal processing operation. This feature of the independent claims, i.e.,

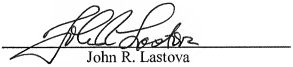
use of the same system bus and the same memory for both the normal operation and the save and restore operation, is not addressed in the Examiner's obviousness objection.

The Examiner acknowledges that Woods does not teach the claimed multi-bit wide system bus and seeks to draw this teaching from Langford. Langford discloses multi-bit address and data buses 14, 16, but as described above, these are used during boundary scan testing to communicate with an external test processor and not with the memory which is used during normal operation. Thus, even if the combination of teaching suggested by the Examiner were made, this combination would not result in a teaching of at least a multi-bit wide system bus transfers "multi-bit data words between said circuit and said memory ... during normal processing operation of said circuit and said memory."

The application is in condition for allowance. An early notice to that effect is requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 
John R. Lastova
Reg. No. 33,149

JRL:maa
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100